CMS

We are at a special time in the life of the experiment: we are defining how our detector will have to be upgraded to exploit correctly the upgraded LHC accelerator performance after 2025

High Luminosity LHC

- In 2012 the European Council defined the priorities for the medium term future of European HEP to be the full exploitation of the LHC complex, through upgrading the Accelerator complex to be able to reach instantaneous luminosities in excess of 10^{35}
- Such luminosities would imply prohibitive experimental conditions and very fast beam burnout, so in practice the future upgraded machine will be one with lumi levelled at 5-7 10^{34} allowing lumi accumulation of several hundreds of fb^{-1} per year
- The P5 committee in the US last year defined the HI Lumi LHC as the priority of the US HEP frontier program

2010 - 2035

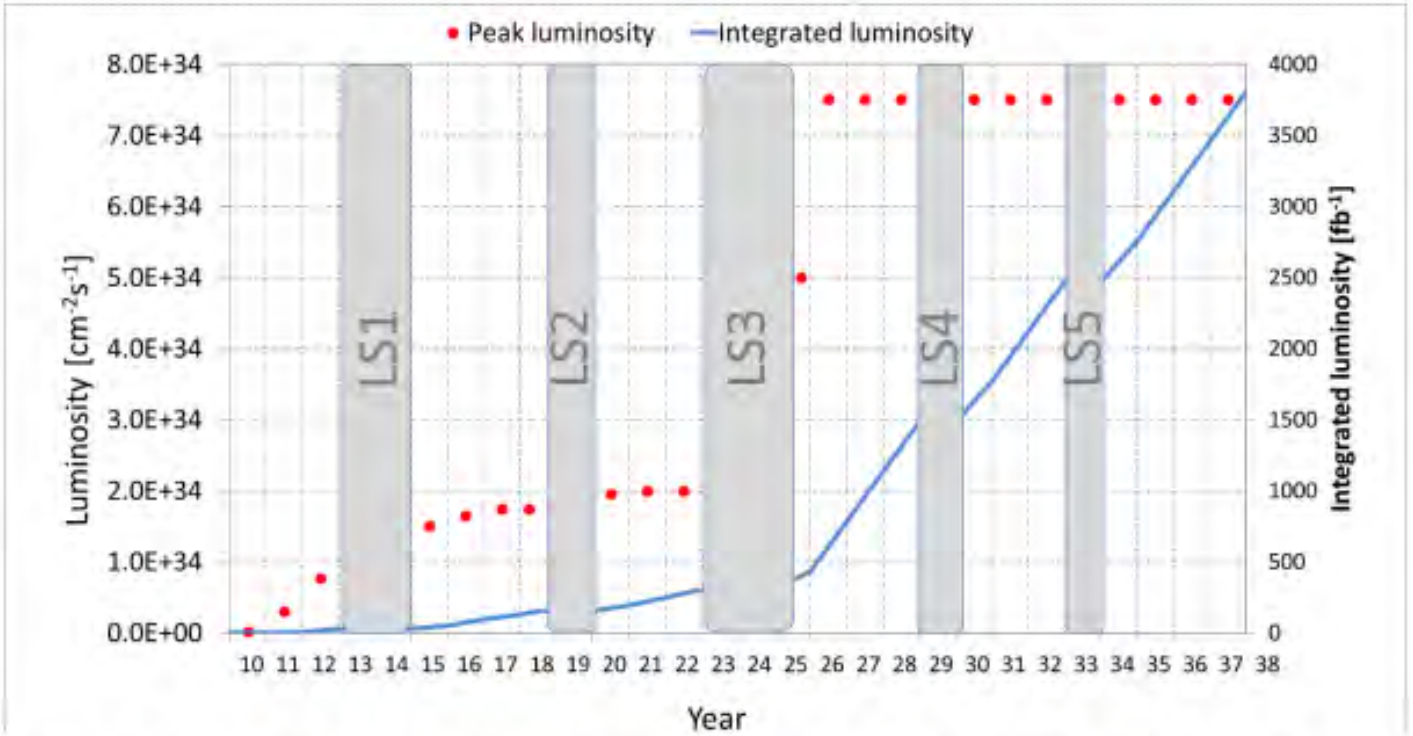
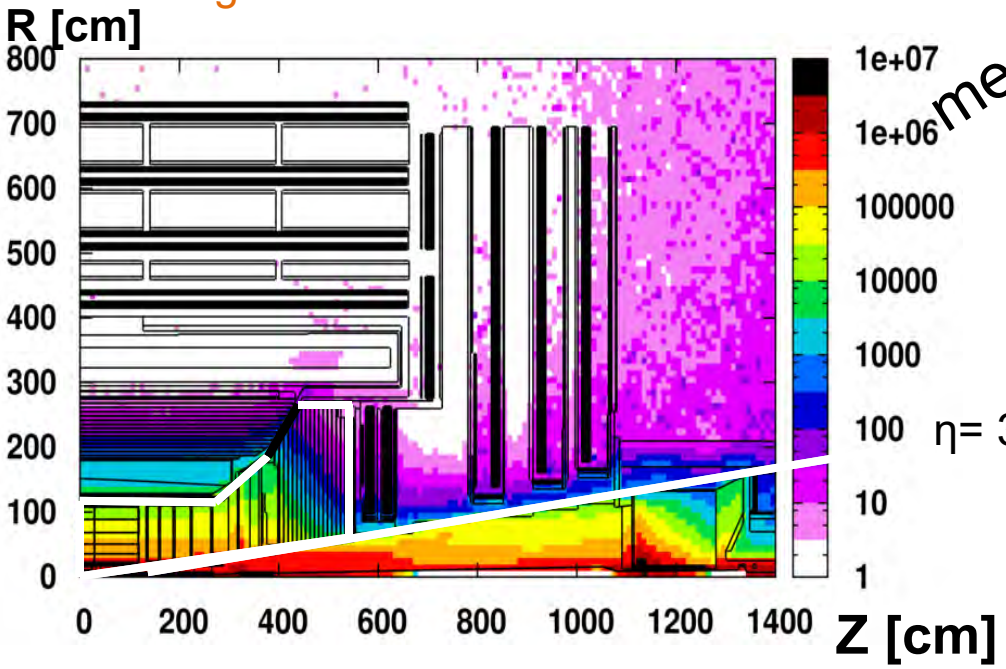


Figure 8: Forecast for peak luminosity (red dots) and integrated one (blue line) in the HL-LHC era, for the case of ultimate HL-LHC parameters. Note that for sake of simplicity there is no learning curve for the luminosity after LS3.

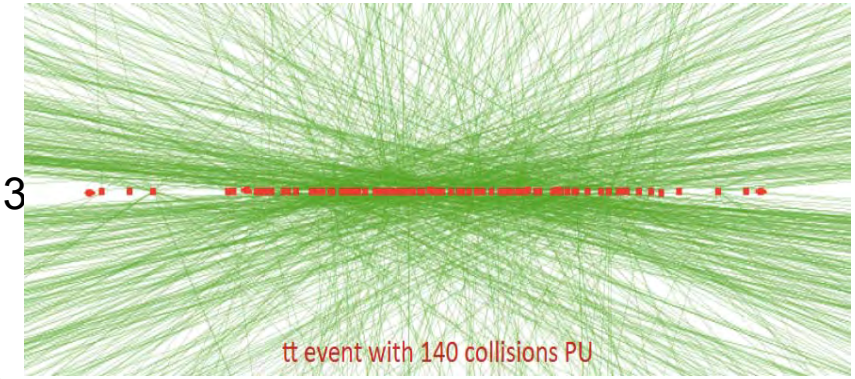
High Lumi LHC challenges

High radiation level



High Pile-Up

ttbar event with 140 PU collisions



Annual dose in HL-LHC will be similar to total dose from LHC start to LS3

→Aging studies show that Tracker & Endcap Calorimeters need replacement

Maintain detector performance in the presence of higher pileup (PU)

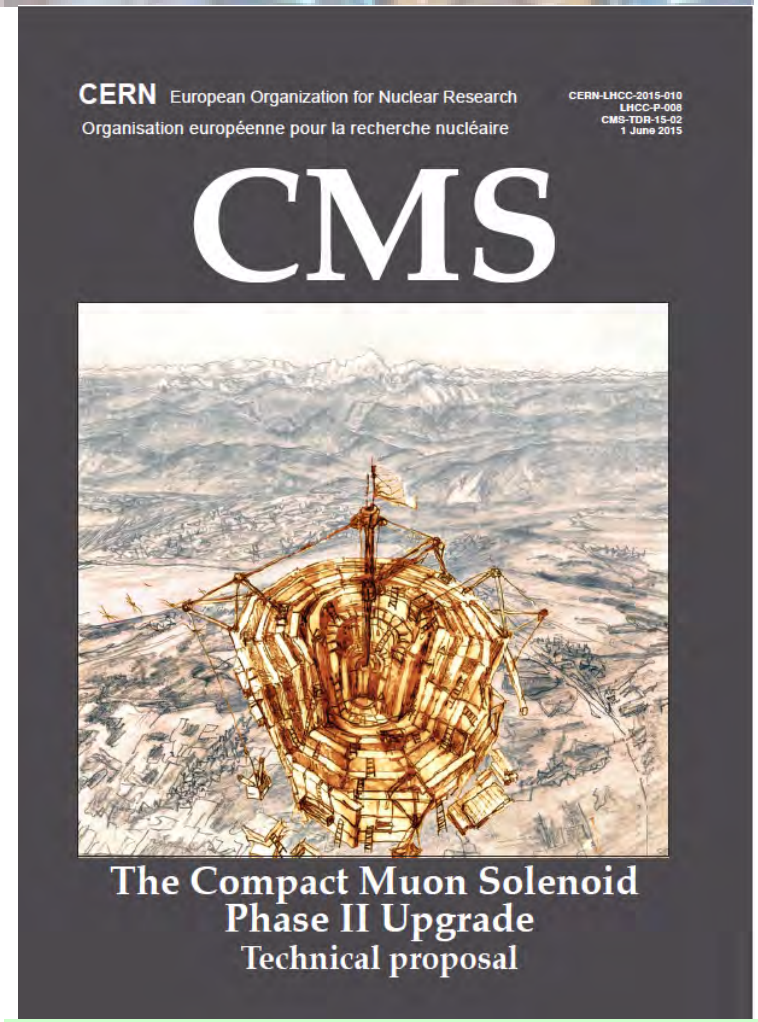
→ Upgrade several detector components

→ Redesign some electronics, trigger and DAQ

CMS Phase II upgrade

- Brief Physics Motivation
- Detector Upgrades
- Physics Object Performance
- Summary & Conclusions

Performance results are assessed using full simulation. The overall goal is to maintain similar physics performance at luminosity of 5 10^{34} Hz/cm^2 as we have at 10^{34} Hz/cm^2 and be able to exploit without too much degradation up to 7.5 10^{34} Hz/cm^2



CERN-LHCC-2015-010https://cds.cern.ch/record/2020886

Baseline upgrade proposal

Muon System
- new DT FE electronics, CSC FEBs in inner rings
- extended η region (GEM & iRPC)
- investigate Muon-tagging up to η ~ 3

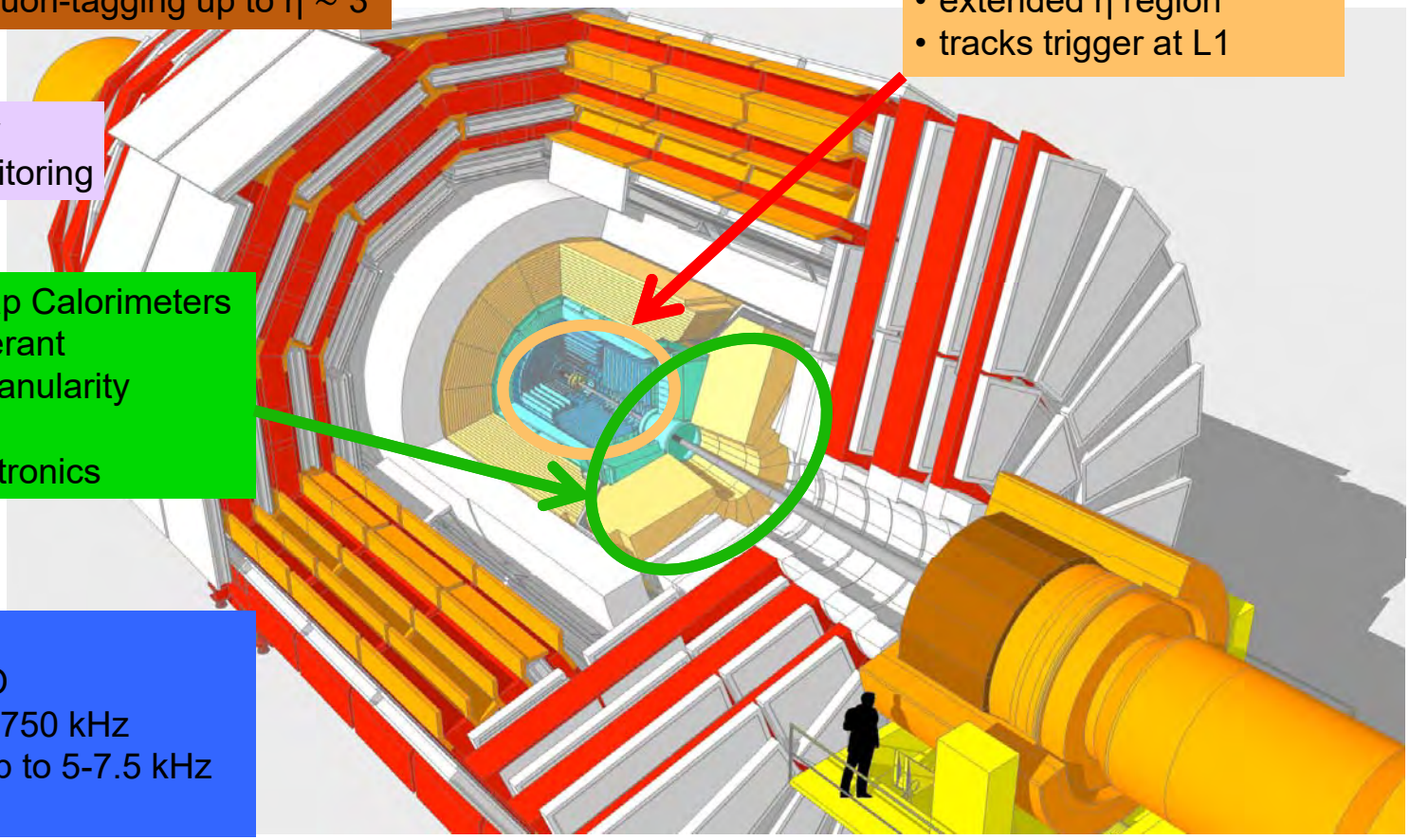
Tracker
- higher granularity
- less material
- better p_T resolution
- extended η region
- tracks trigger at L1

New luminosity and beam monitoring

Replace Endcap Calorimeters
- radiation tolerant
- increased granularity

Barrel ECAL
- new FE electronics

Trigger/DAQ
- new FE & RO
- L1 up to 500-750 kHz
- HLT output up to 5-7.5 kHz
- tracking @L1

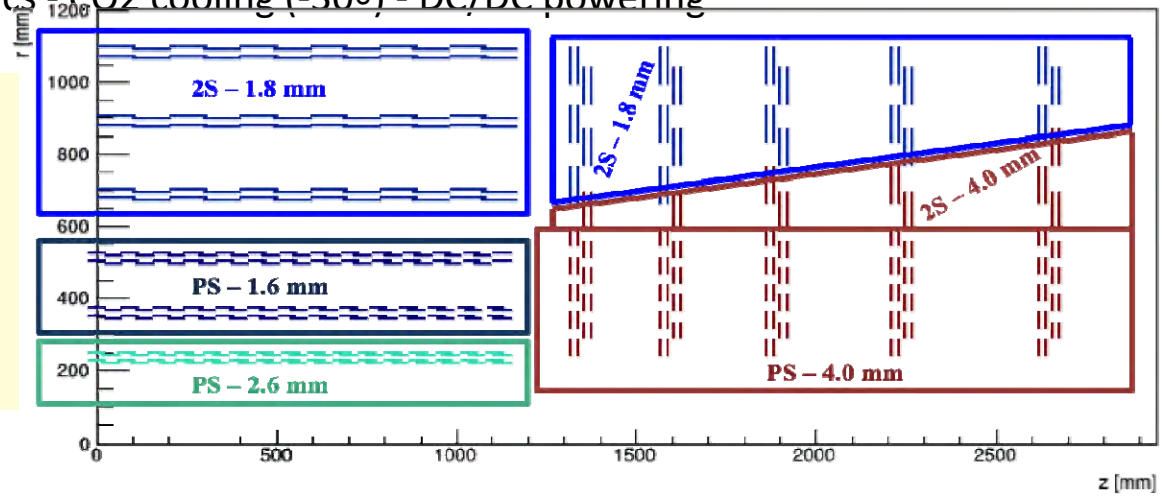


Outer tracker upgrade

Several configurations investigated with simplified simulation to define baseline:

- 6/5 barrel/endcap layers/disks - instead of 10/11 in current OT
- Increased granularity through short strips - ≃ x 4 current OT
- 2 sensors modules in all layers for Trigger purpose
- Long Pixel in 3 inner layer modules (PS) for z-coordinate measurement
- Light module design & mechanics - CO2 cooling (-30◦) - DC/DC powering

Total Outer Tracker
- 220 m^2 area - 15500 modules
- 50M strips - 220M macro-pixels
- 90/100 µm pitch (2S/PS modules)
- 2.5/5 cm strips (2S/PS) - 1.5 mm macro-pixels in PS modules
- 200 µm active or physical thickness

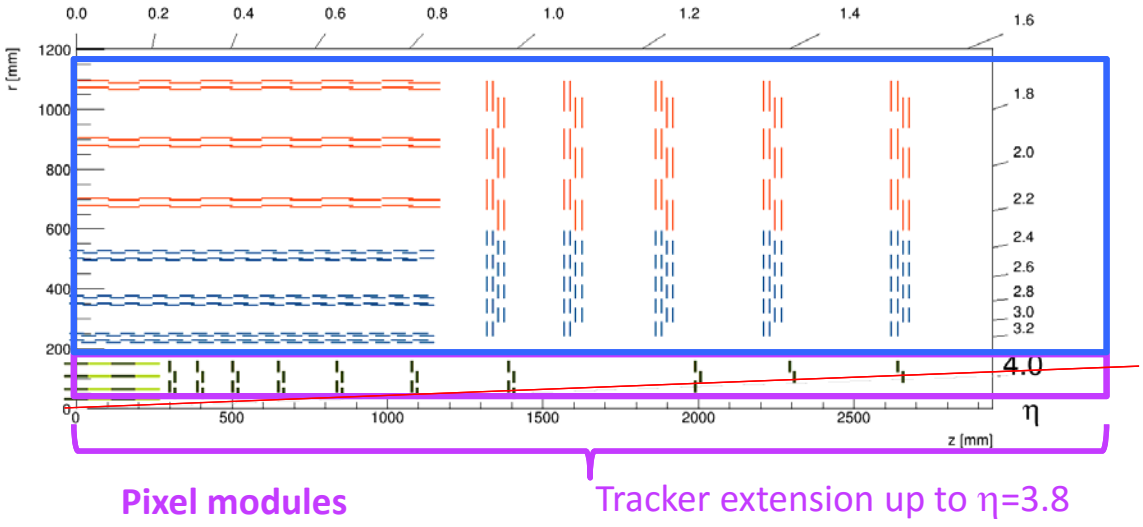


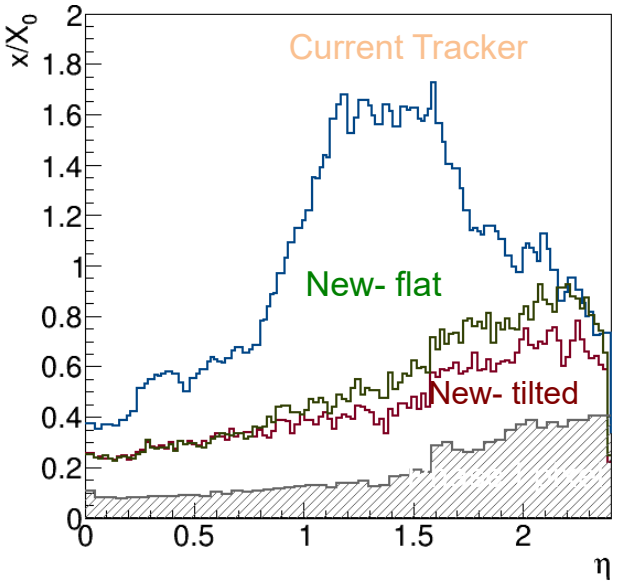
Ongoing study of alternative design with tilted modules in PS layers
- Further reduce material and number of modules

Pixel upgrade

Current configuration based on Phase-I design - ongoing studies to reduce material and to improve/adapt resolution through reduced pixel size

- Barrel pixel with 4 layers at 3, 7, 11 and 16 cm
- Forward pixel with 10 disks extending coverage to η = 3.8
- Data readout at 750 kHz
- Maintainable during winter shutdown





Material (lighten up!)

- Tracker weight ½ of current
- Improved track p_T resolution & reduce rate of γ conversion (factor 2 to 3 depending on η)
- ex. HH -> bbγγ; ttH -> γγ ; H -> μμ - $B_{s,d}$ -> μμ ..

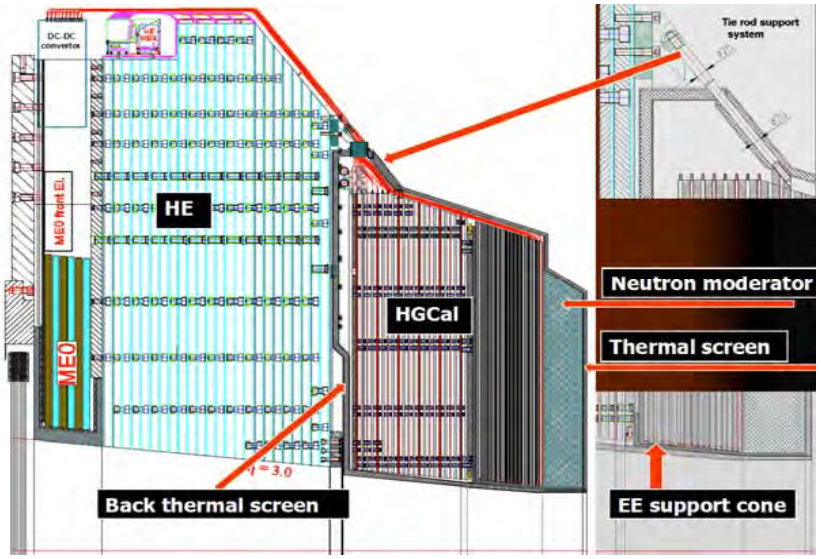
Total pixel area ~ 4.0 m^2

- 50x50 - 25x100μm^2 pixels
- ≤ 150 μm sensor physical thickness

Endcap calorimeter upgrade

- 3D shower measurement in High Granularity Calorimeter (HGC)
  - Electromagnetic EE (Σ_{depth}~26 X_0, 1.5λ): 28 layers of Silicon-W absorber
  - Front Hadronic FH (Σ_{depth}~3.5 λ): 12 layers of Silicon/Brass
- Back Hadronic Calorimeter (BH) (Σ_{depth}~5 λ): 12 layers of Scintillator/Brass

Total Depth >10λ



EE: 380 m^2 - 4.3 Mch - 13.9k modules - 16t
FG: 209 m^2 - 1.8 Mch - 7.6k modules - 36.5t
BH: 428 m^2 - 5184 SiPMs

ΔE/E ~ 20%/√E; 3D shower reconstructio
- **Use shower topology to mitigate PU effect**

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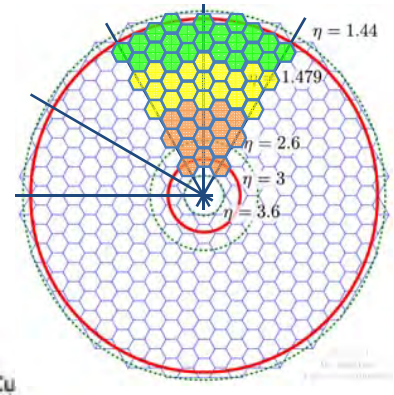
Some details about readout

sensors: three active thicknesses 100-200-300 μm
0.5(1) cm^2 pads for 100(200/300) μm



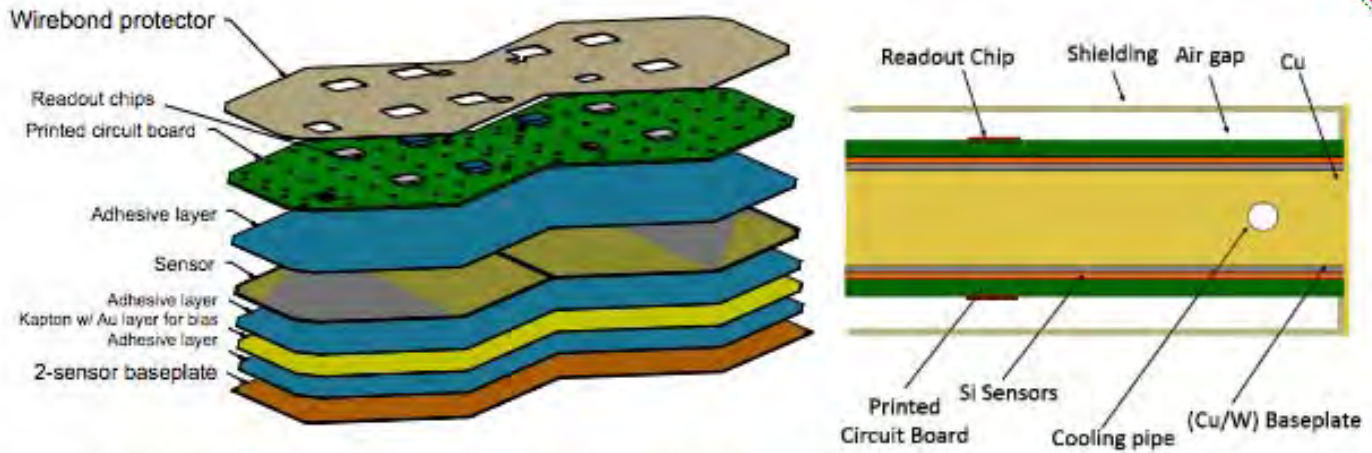
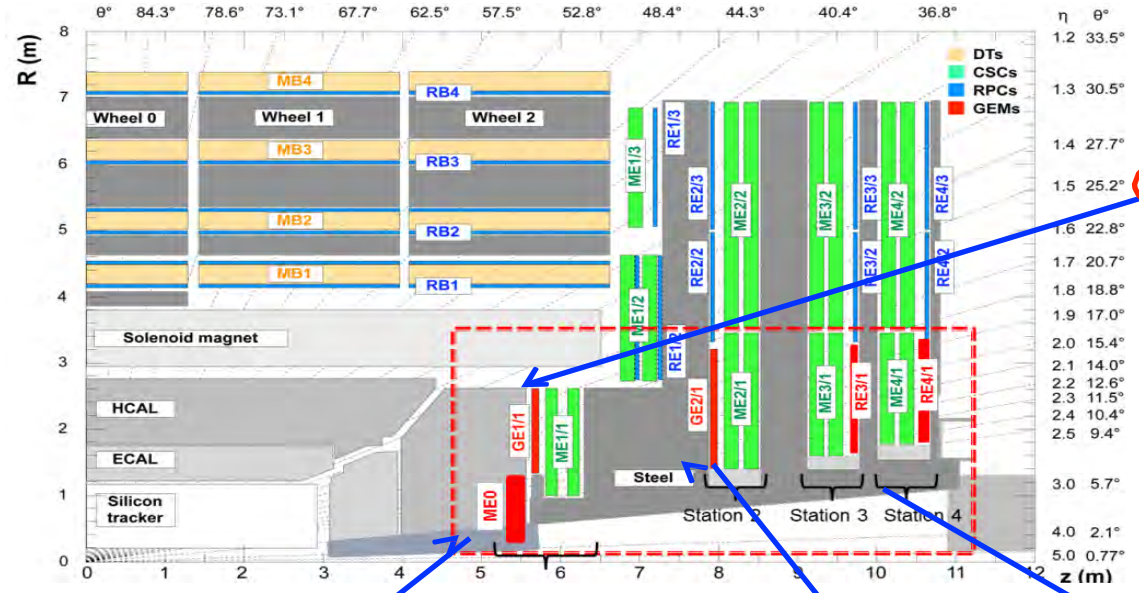
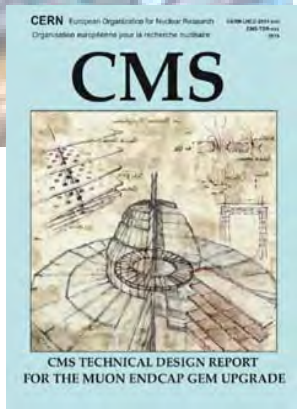


Figure 3.25: (Left) Module, consisting of printed circuit board, silicon sensors, and baseplate. (Right) Sketch of modules mounted either side of a copper and tungsten absorber/cooling plate, showing the longitudinal arrangement of a double layer.

Forward Muon System





CERN-LHCC-2015-012

GE1/1:

Trigger and reconstruction

- **1.55 < |η| < 2.18**
- baseline detector for GEM project
- 36 staggered super-chambers (SC) per endcap, each super-chamber spans 10°
- One super-chamber is made of 2 back-to-back triple-GEM detectors
- **Installation: LS2)**

ME0:

Muon tagger

- **2.4 < |η| < 3.0**

GE2/1:

Trigger and reconstruction

- **1.55 < |η| < 2.45**
- 18 staggered SC per endcap, each chamber covers 20° , 3.5 x GE1/1 area
- Installation: LS3

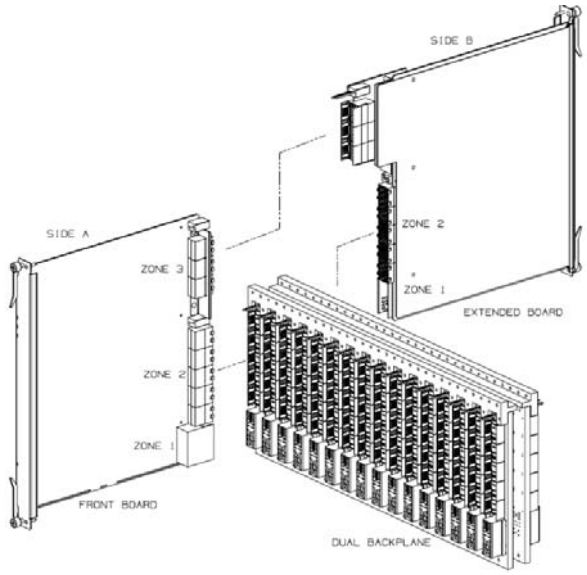
RE 3/1 –RE4/1 :

Trigger and reconstruction

- **1.8 < |η| < 2.4**
- Improved RPC (iRPC), finer pitch
- 18 chambers per endcap, each chamber spans 20°
- Installation: LS3

Digital electronics readout modules

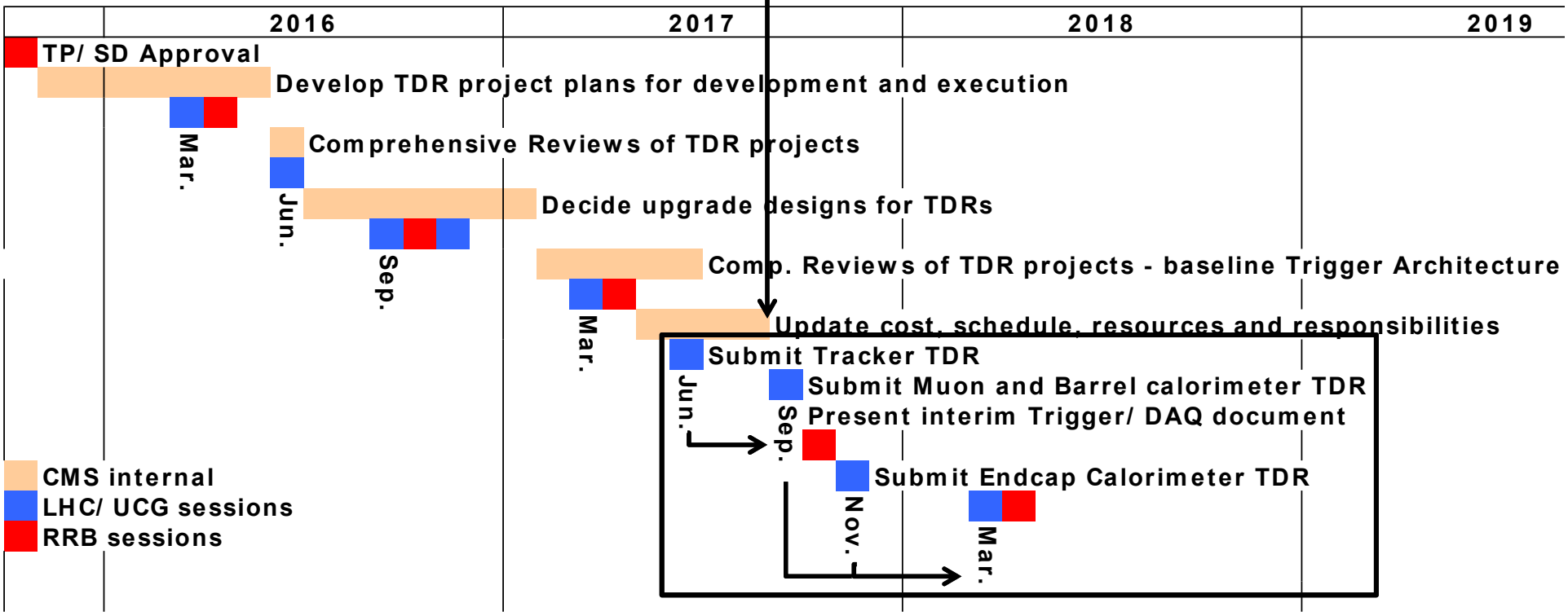
- The upgraded detector will need ~ 1500 electronics board (likely in the A-TCA standard) of various custom design (expect the cost of each board to be < 15000 CHF)
- 



https://www.picmg.org/openstandards/advancedtca/

Next step : Technical Design Reports

Aiming to provide at the same time material on cost, schedule & resources for UCG review for possible endorsements at RRB in Oct. 2017 and Apr. 2018



- Also Common Infrastructure upgrades and LS2-LS3 work document in 2016-17, and Trigger interim document in Sept. 2017
- TDRs for Trigger, DAQ, BRIL in 2019-2020

Timeline

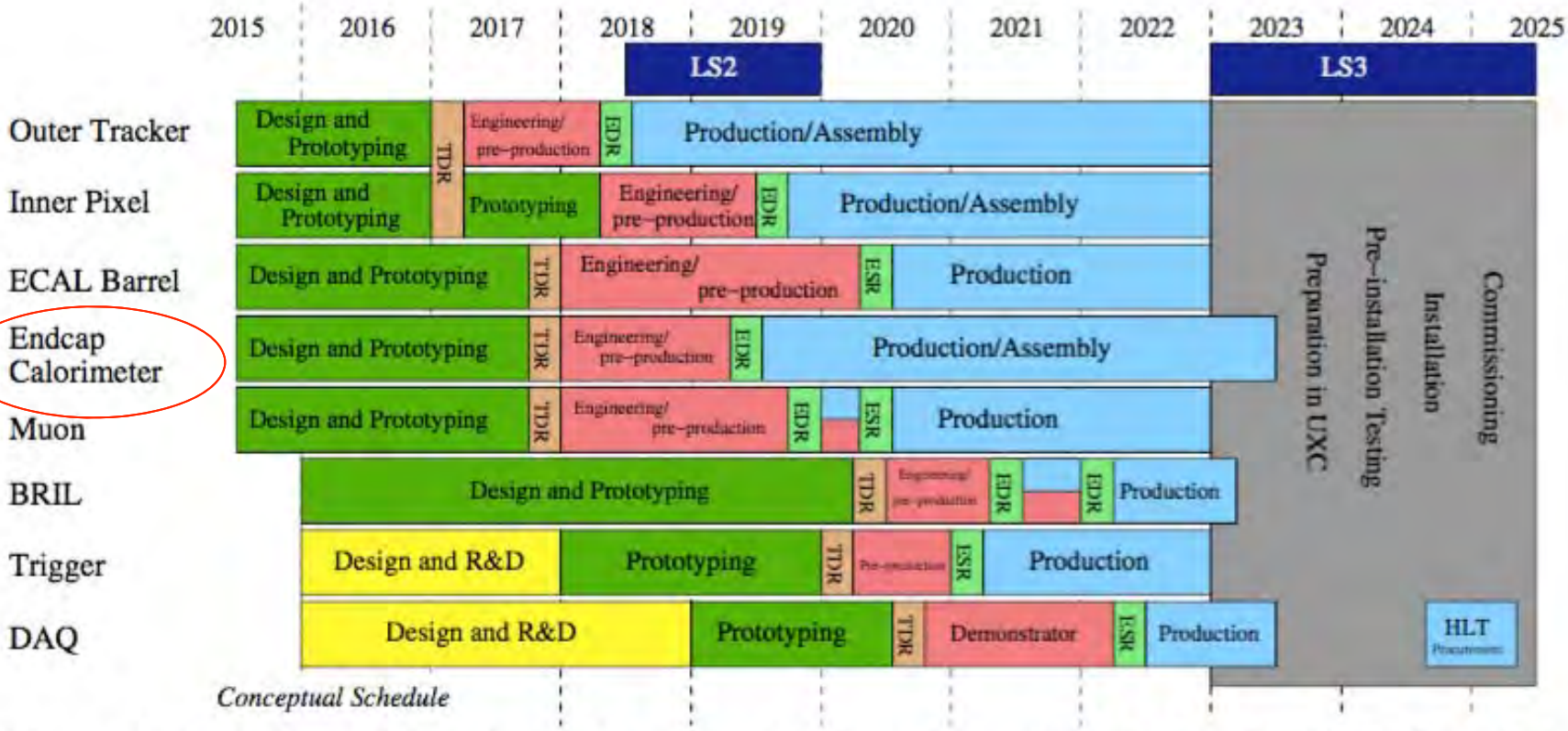


Figure 12.1: Outline of the Phase-II Timeline. Each project will include a detailed schedule in the respective TDR.

‘Core’ Cost Profile

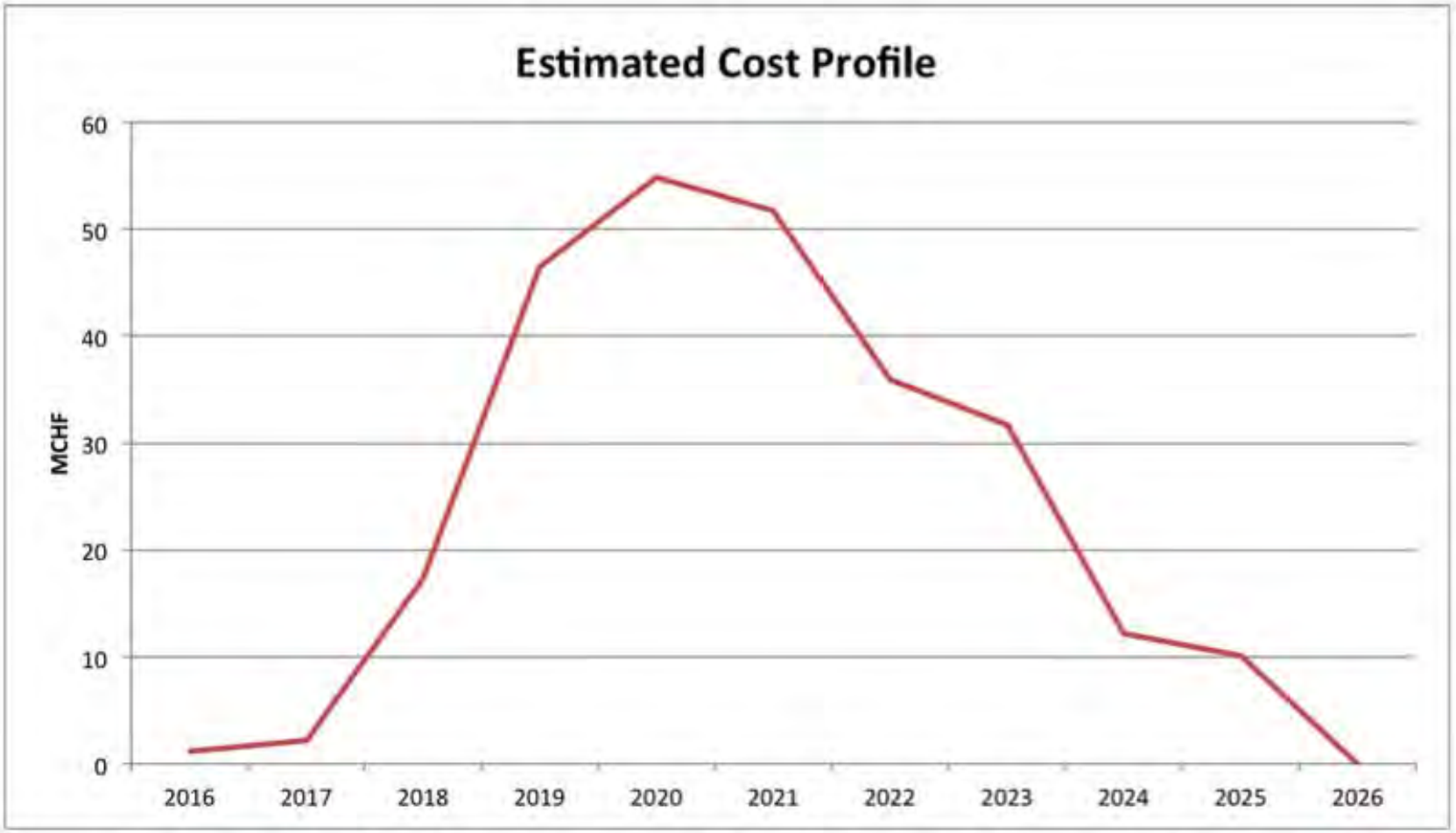


Figure 12.2: Anticipated CORE spending profile with the installation occurring during LS3 in 2023-2025.

Upgrade needs

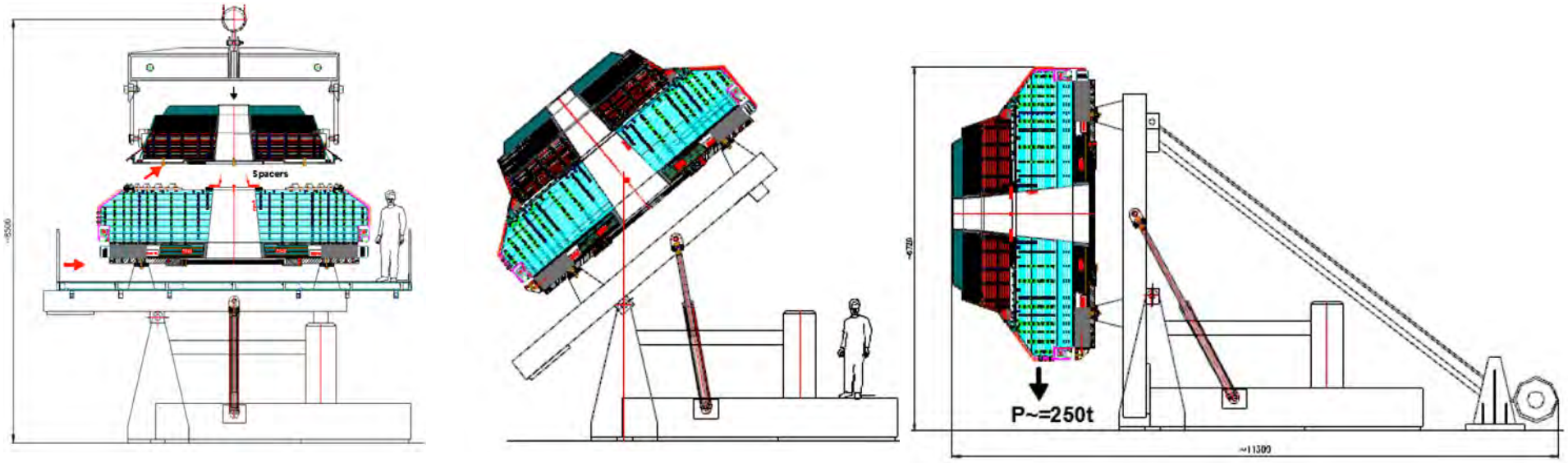
- Today we are not yet in conditions to define in detail the needs in terms of mechanics and electronics: this will be defined in the Technical Design Reports which will be submitted from the end of 2017 onwards
- What we can describe today are the performance we will need and functionally some of the infrastructure we will need

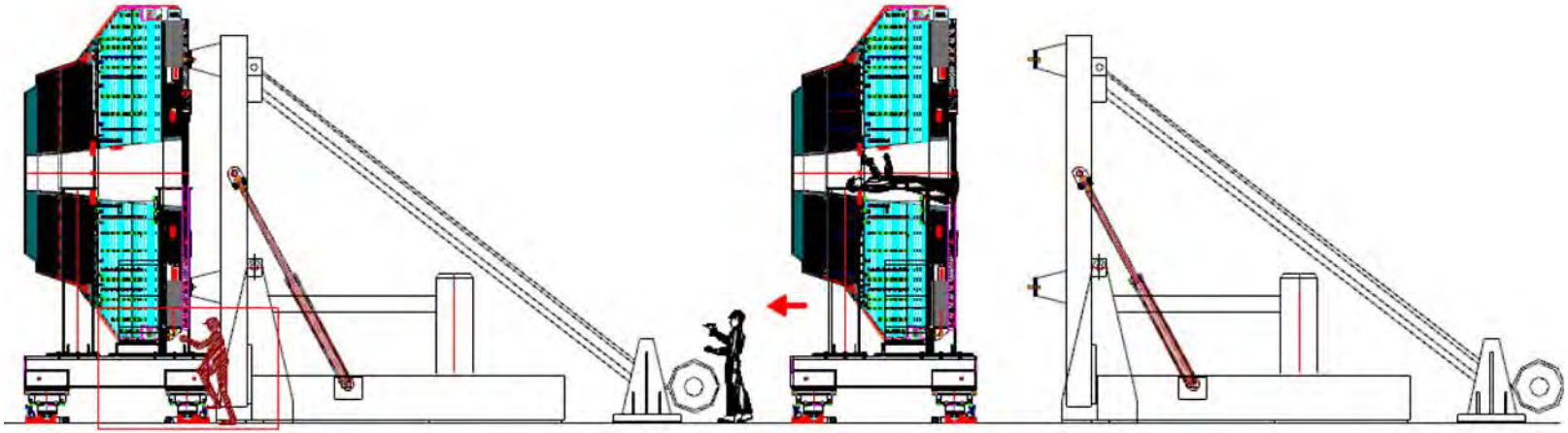
Example: mechanical tools

- In order to manipulate the pieces we will need to take down or install we know that we will need specific tools.
- Some are already available from the time of construction (e.g. the tool to manipulate Barrel Electromagnetic calorimeters modules) and can be adapted to the needs, others will be developed. Sketches of these are in the next slides

Phase II Endcap Calorimeter assembly

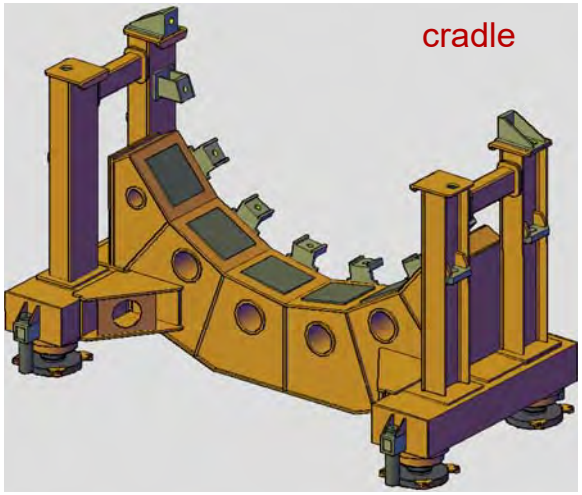
Endcap cal assembled horizontal on tilting table, rotated vertical and transferred to cradle



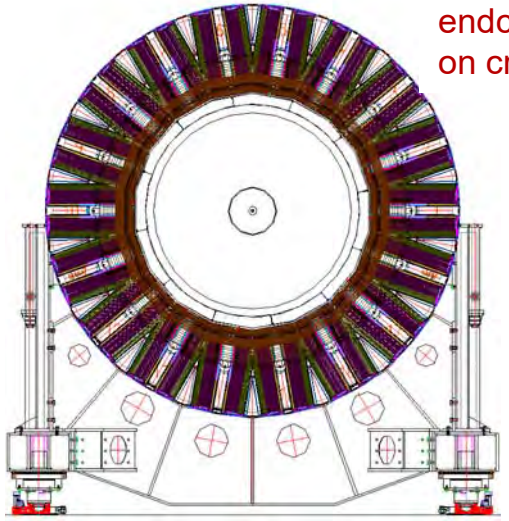


Dismounting/mounting of endcap cal

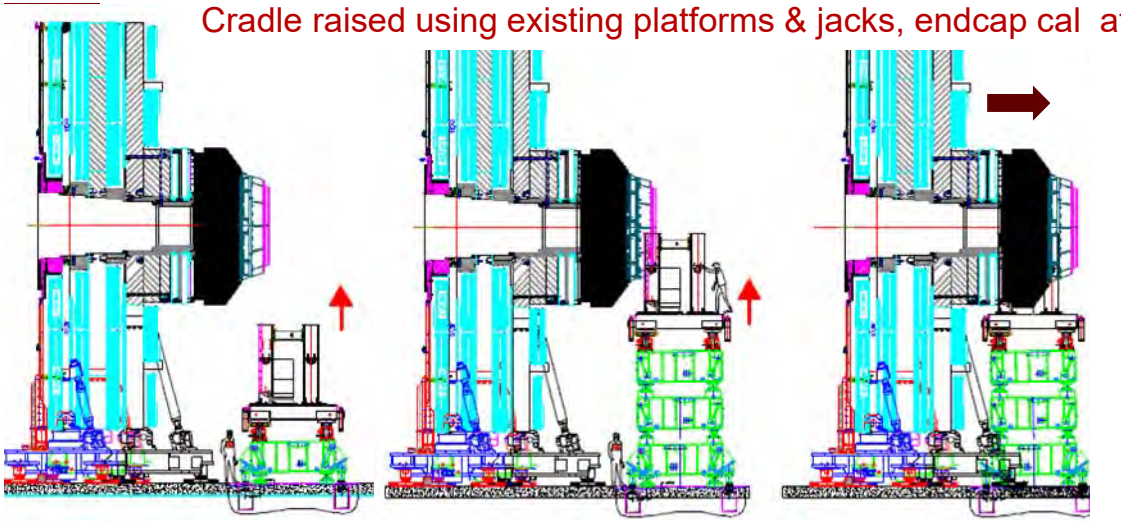
cradle



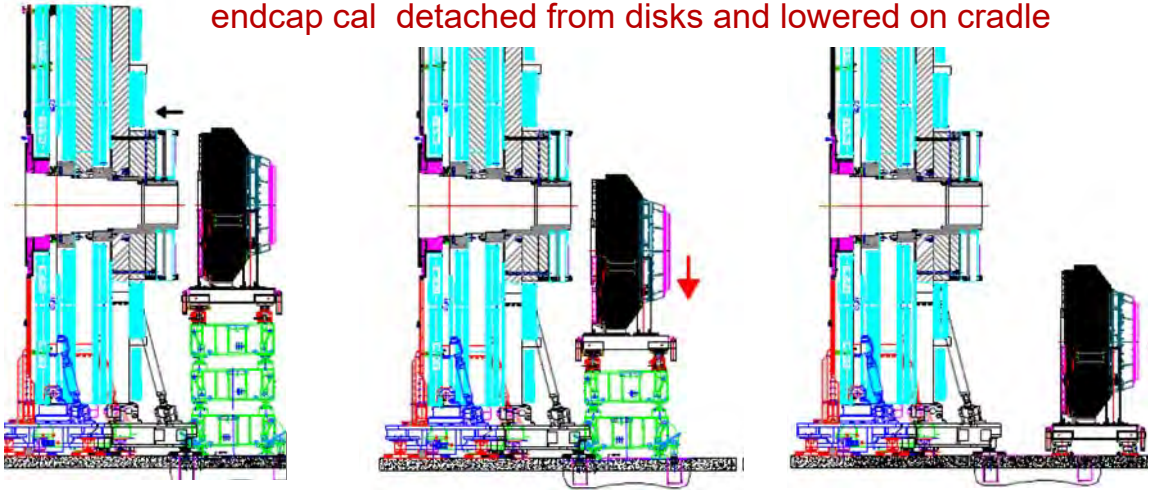
endcap
on cradle



Cradle raised using existing platforms & jacks, endcap cal attache

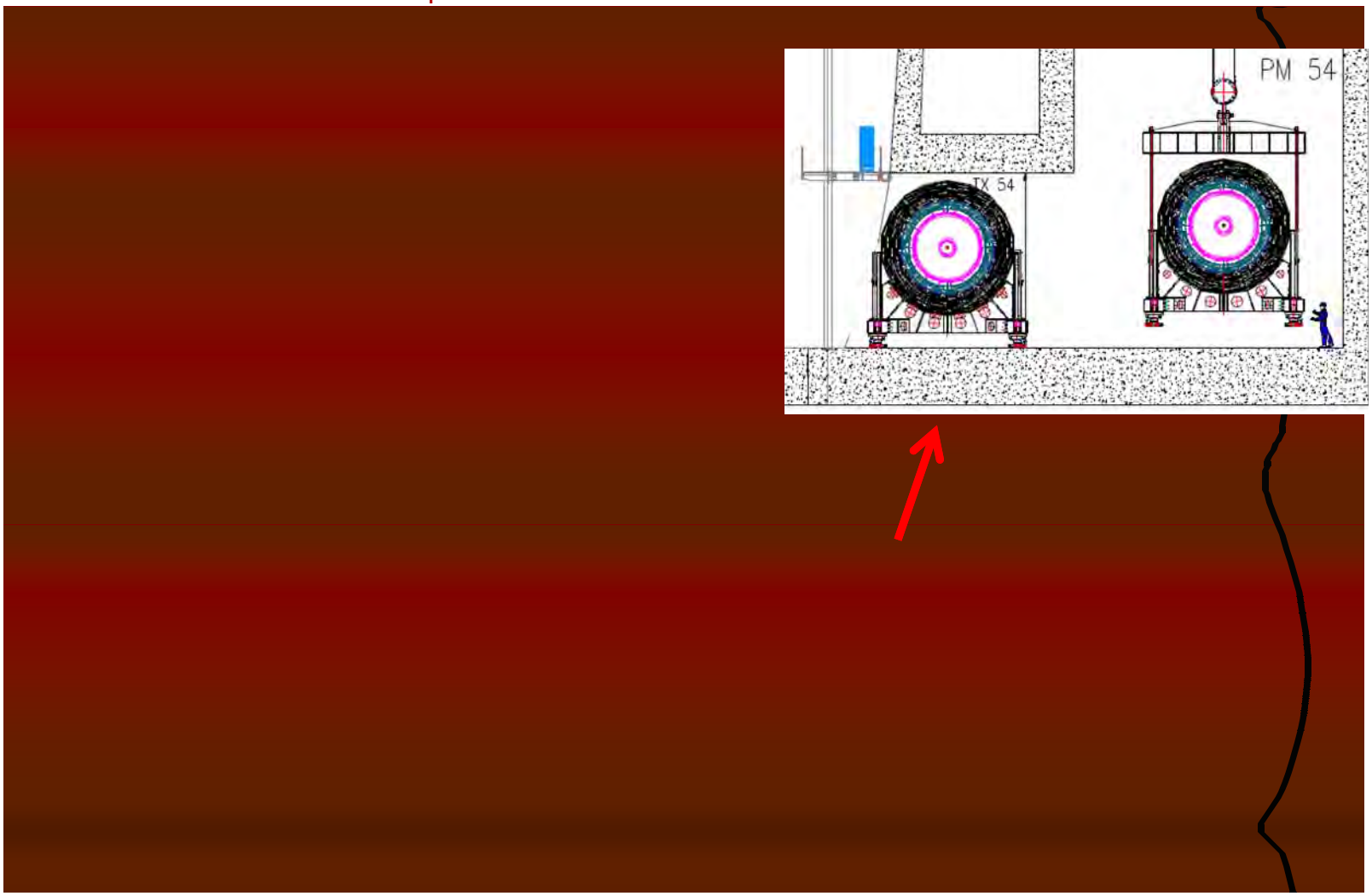


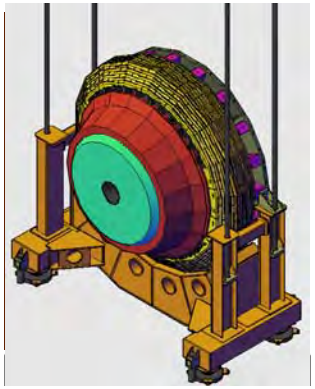
endcap cal detached from disks and lowered on cradle



Endcap calo: cavern to shaft to surface

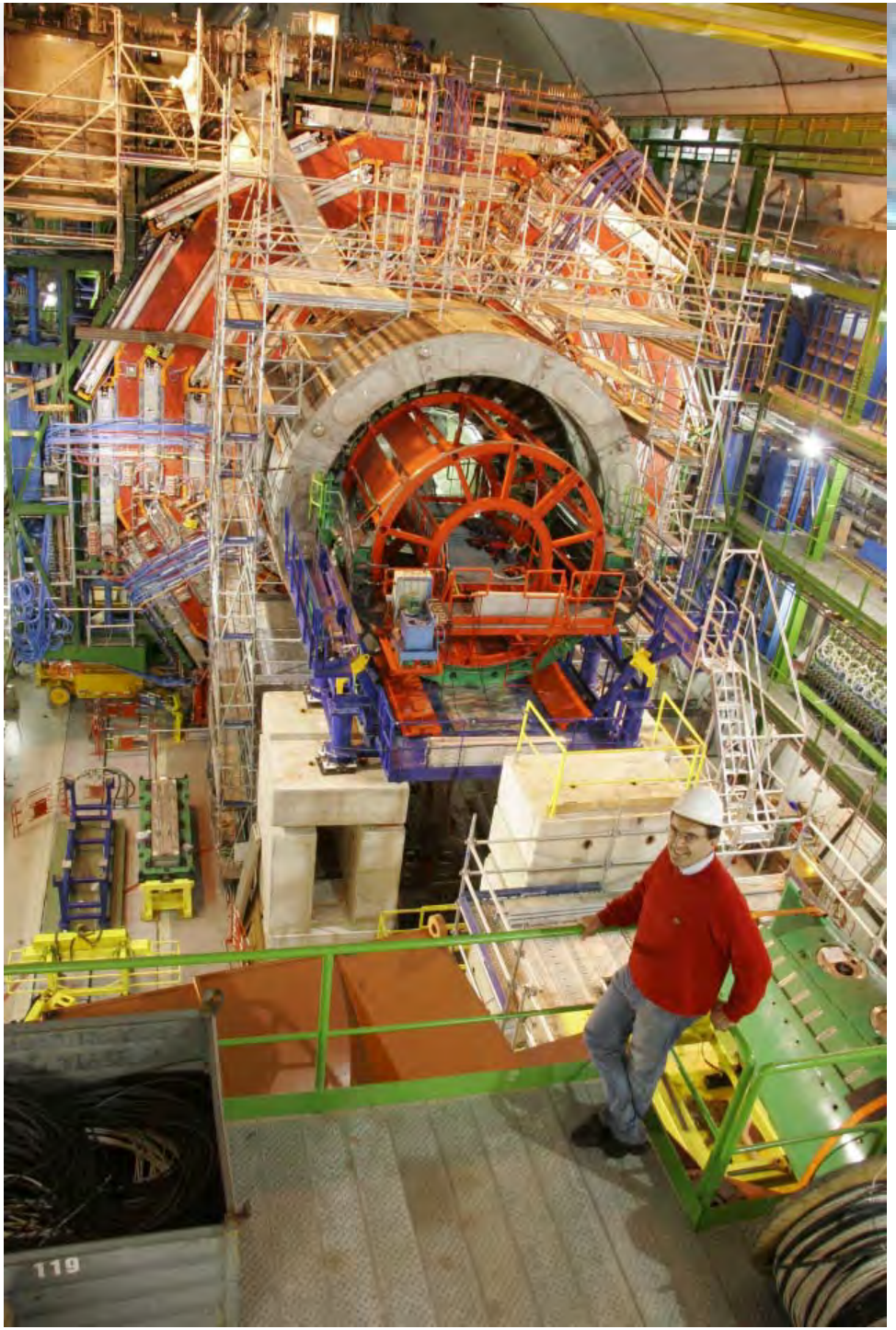
Endcap cal on cradle moved out of cavern and under 100m shaft for transfer to surface





Examples from construction


CONVOI
EXCEPTIONNEL
S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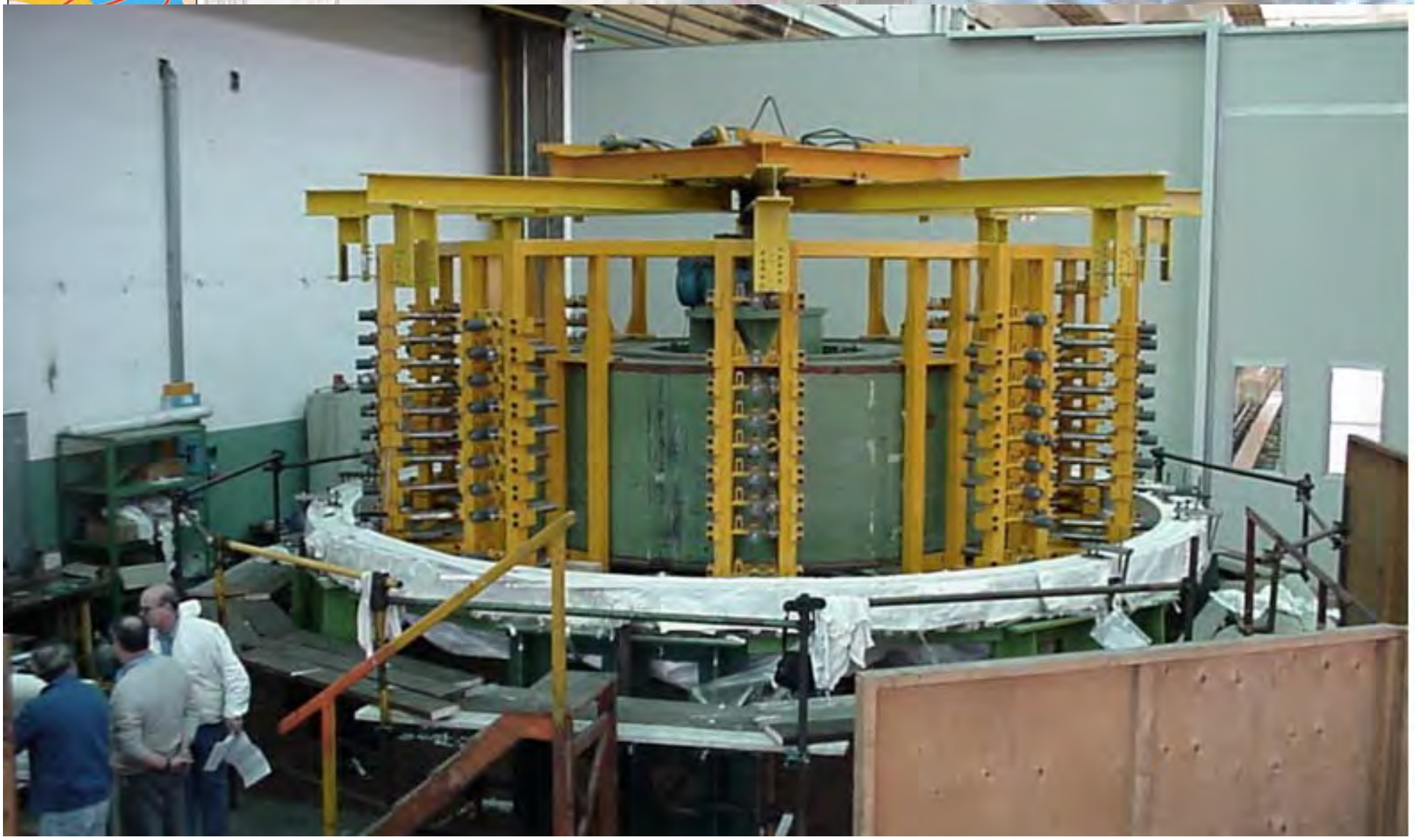
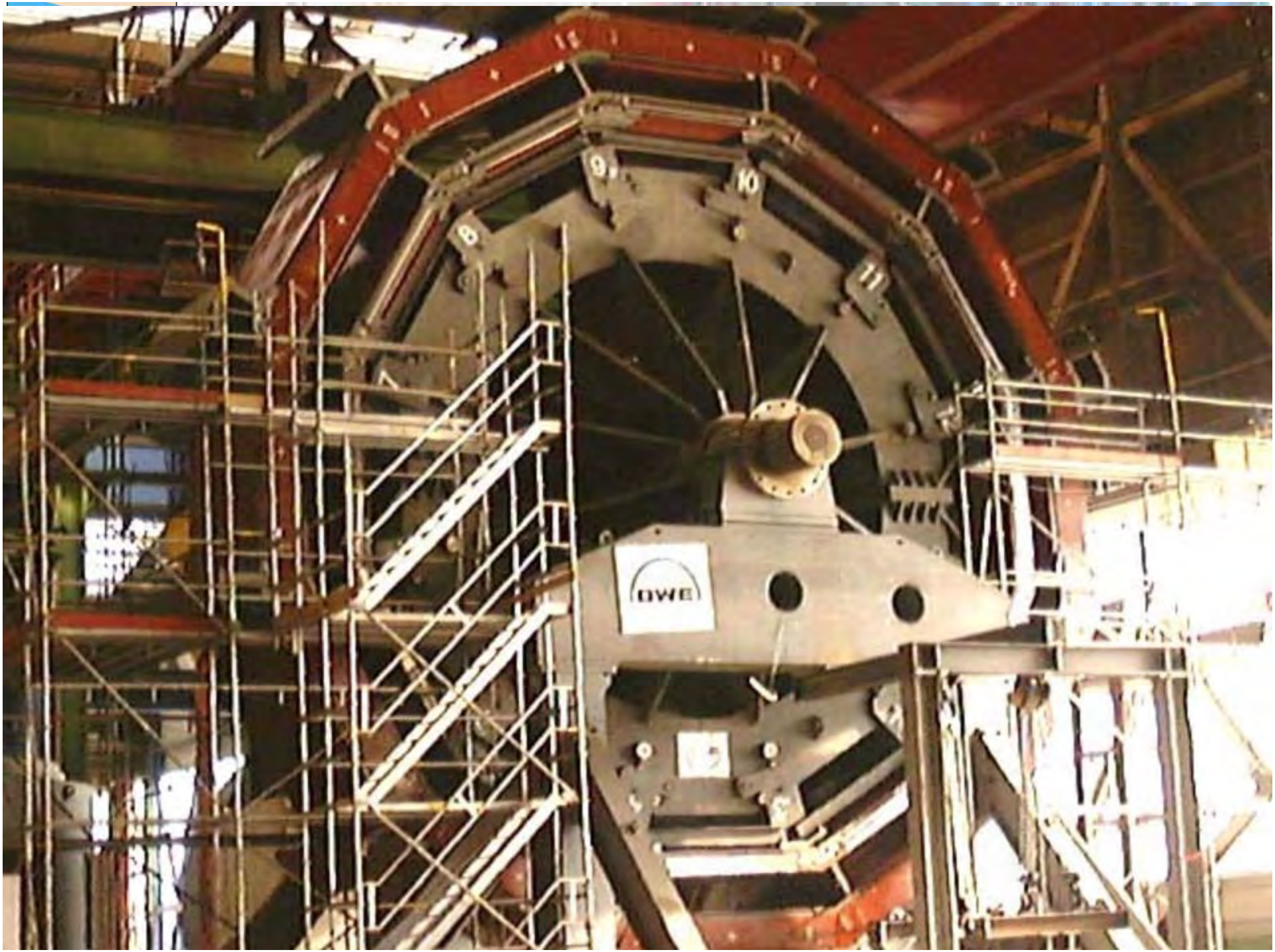
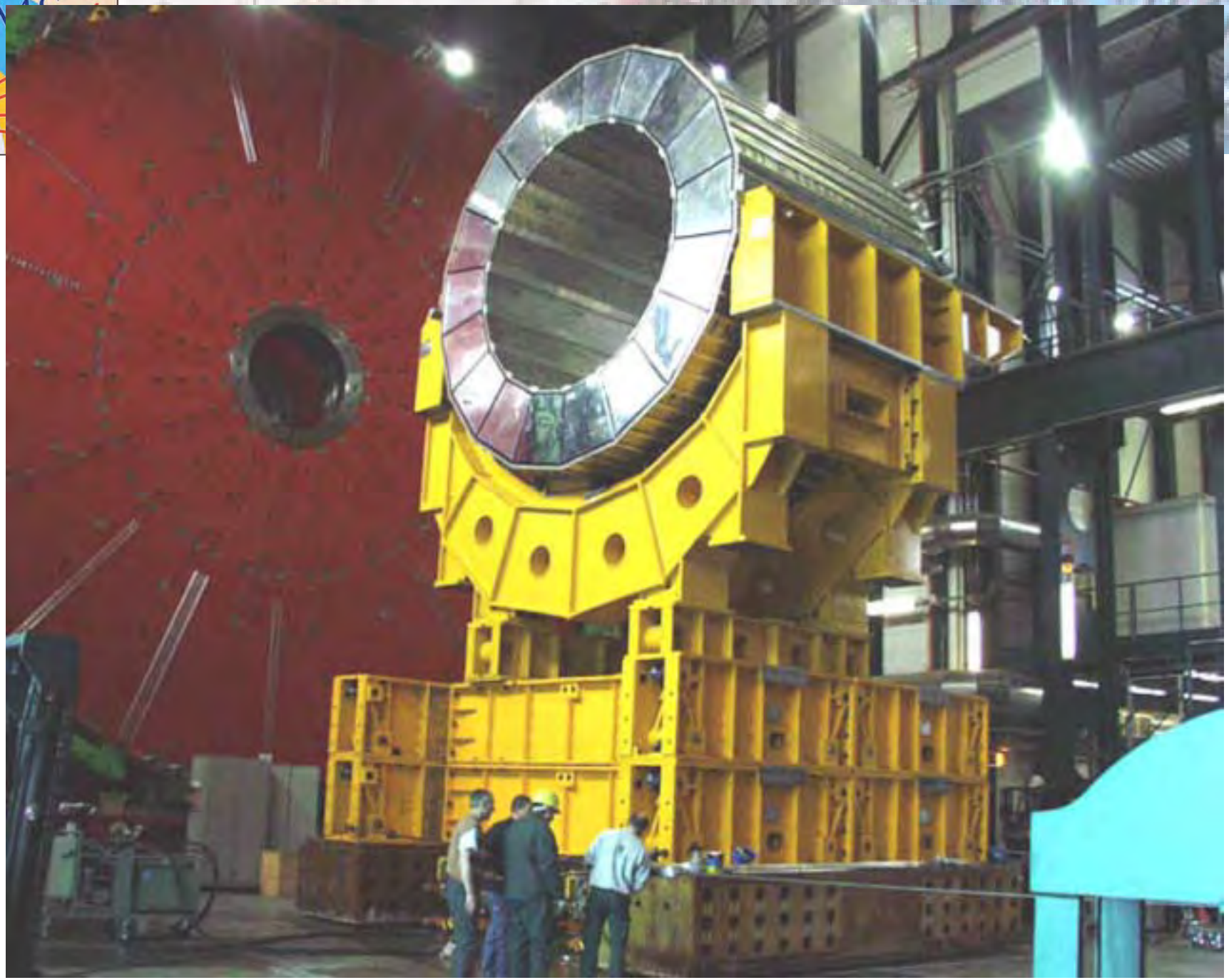


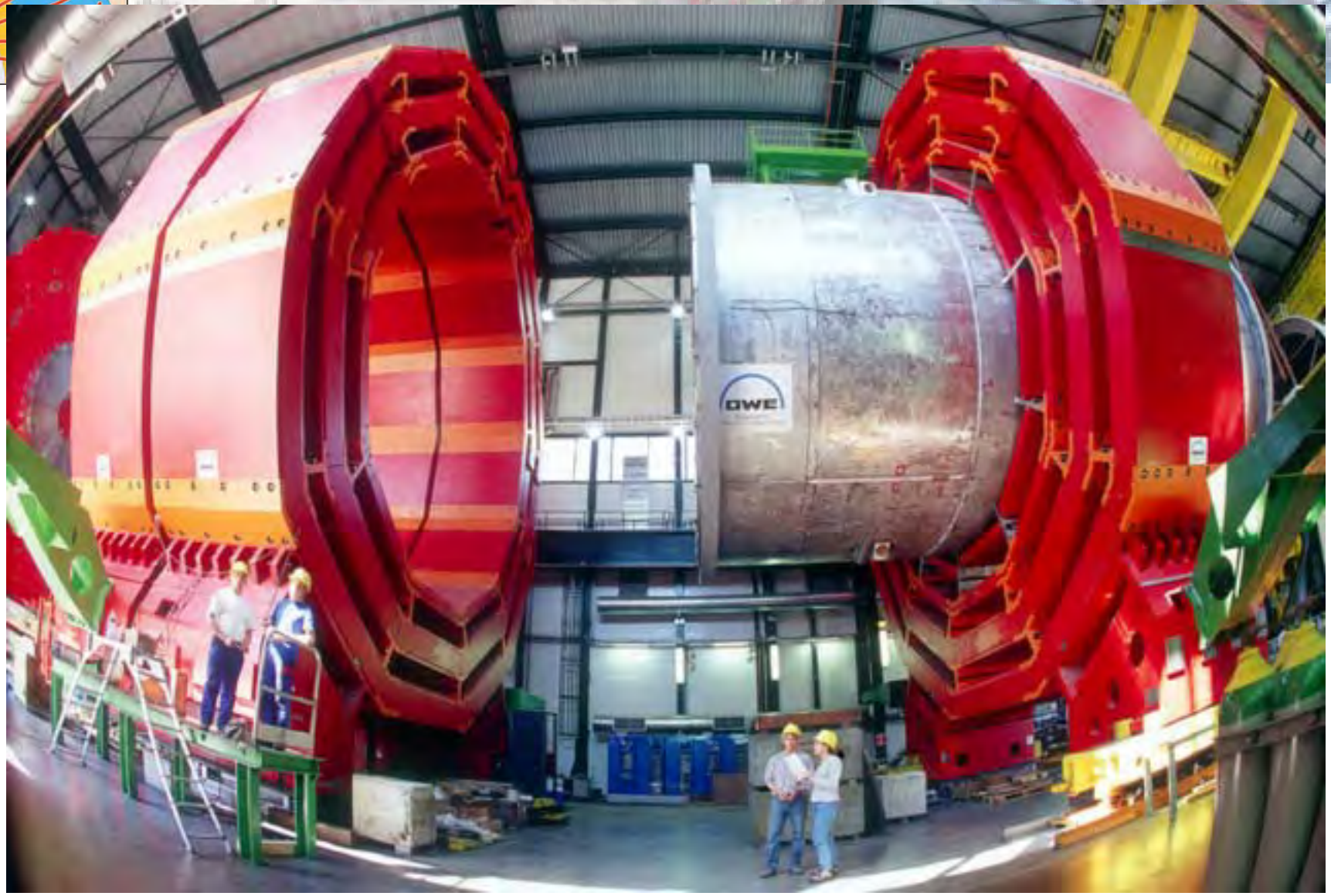

8
9
10
11
DWE


925

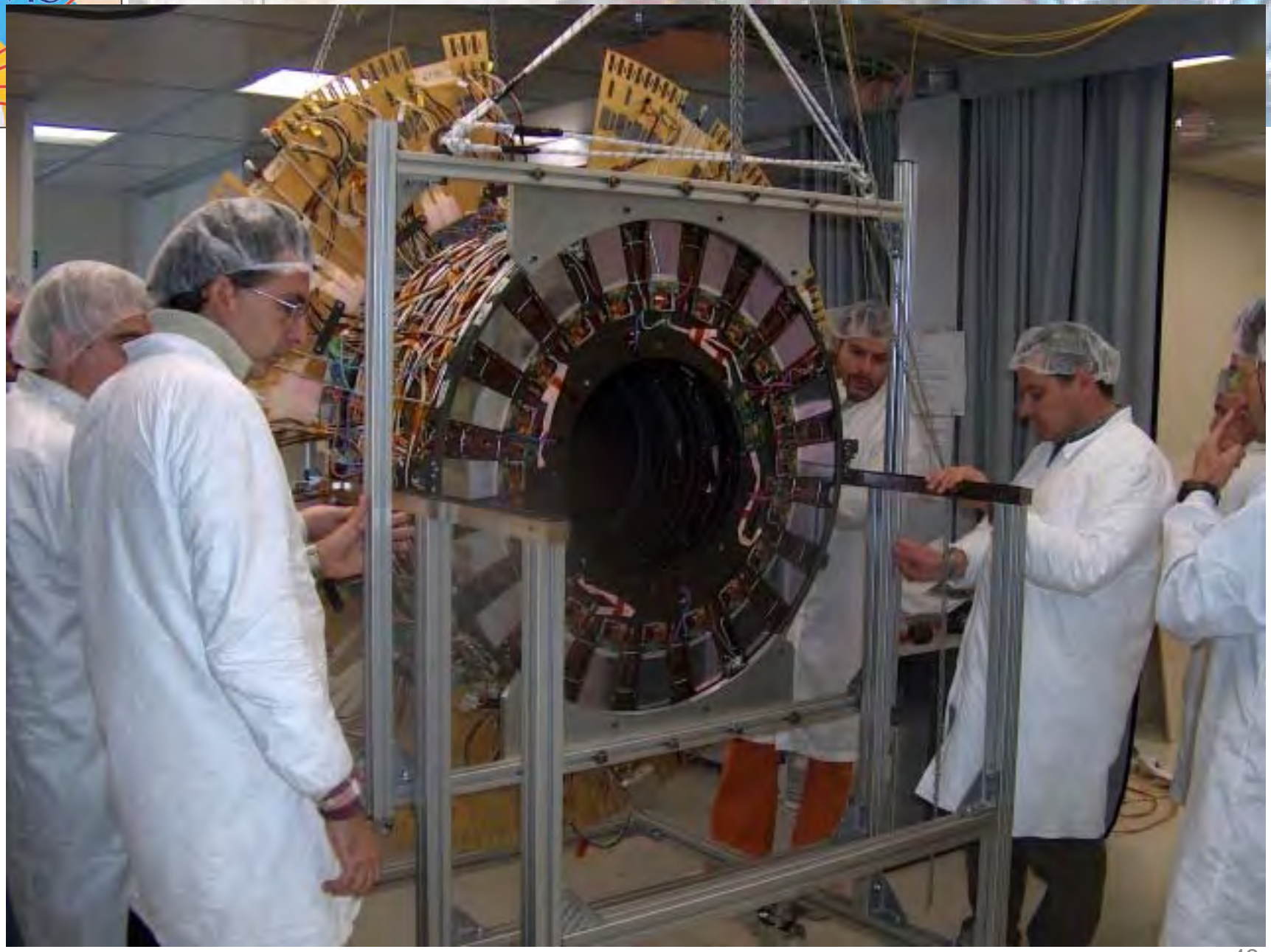

SL 172-18 E2WD
SL 153-12 E 2WD

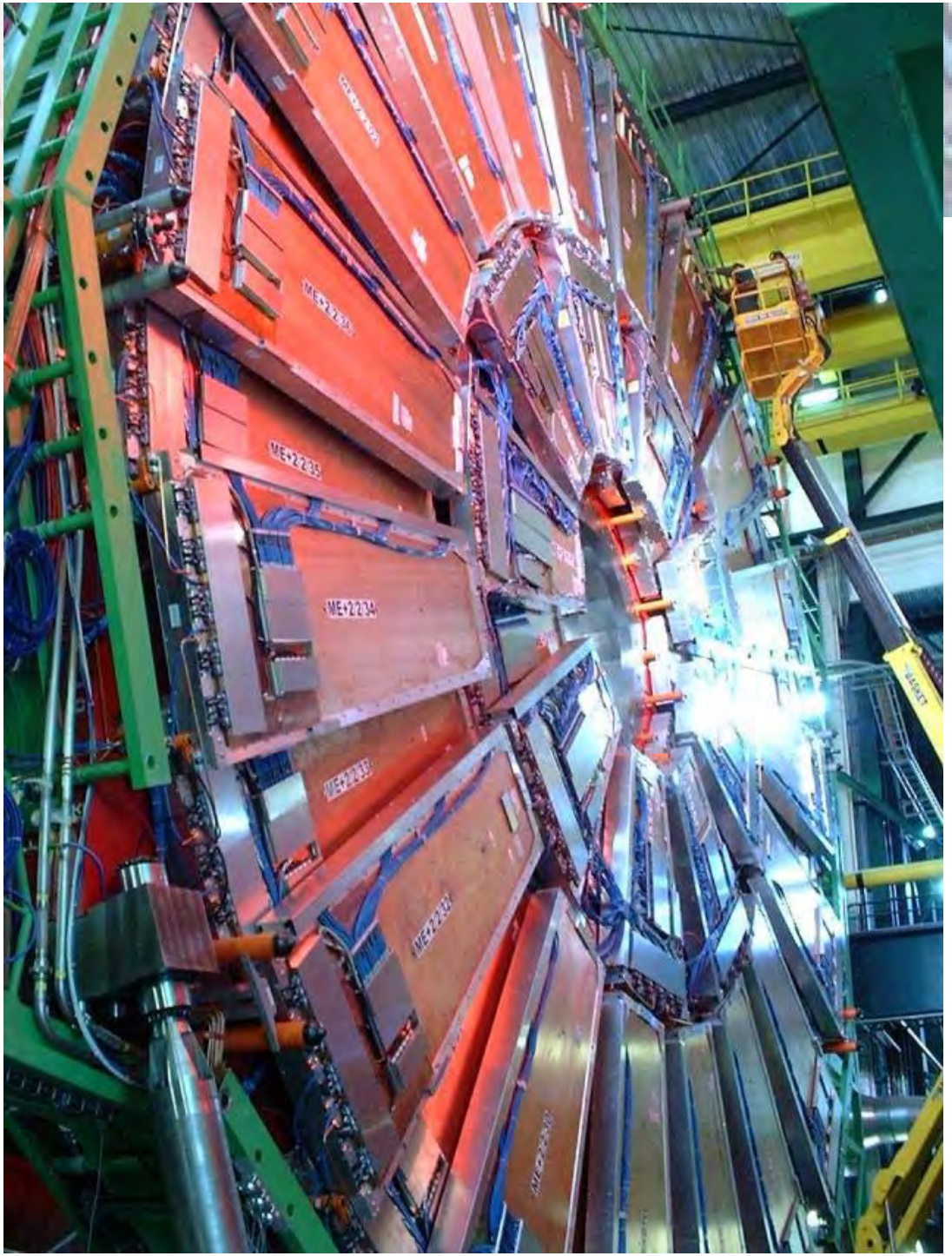


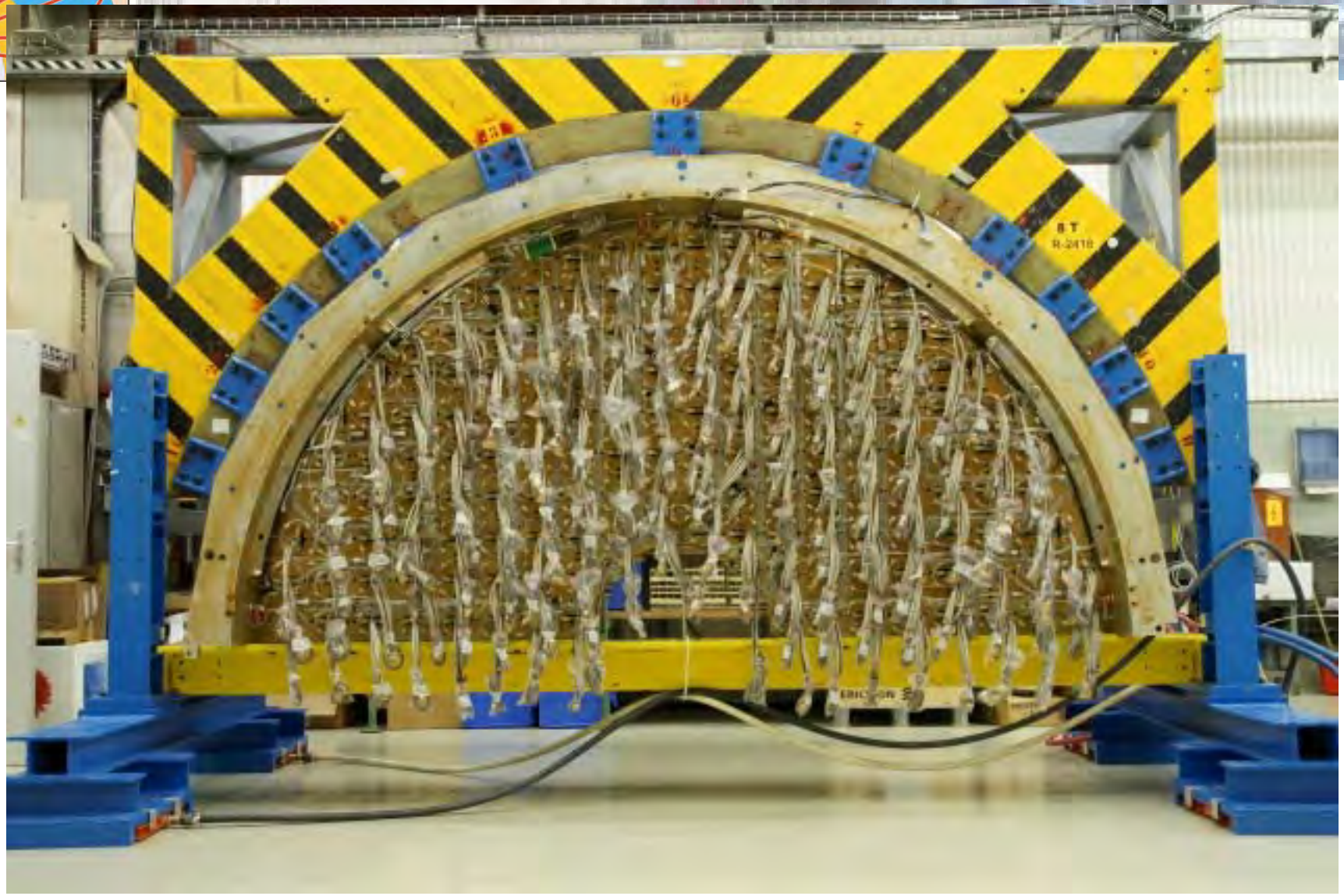

TAIM-TPC
SPAIN
80/5 Tm

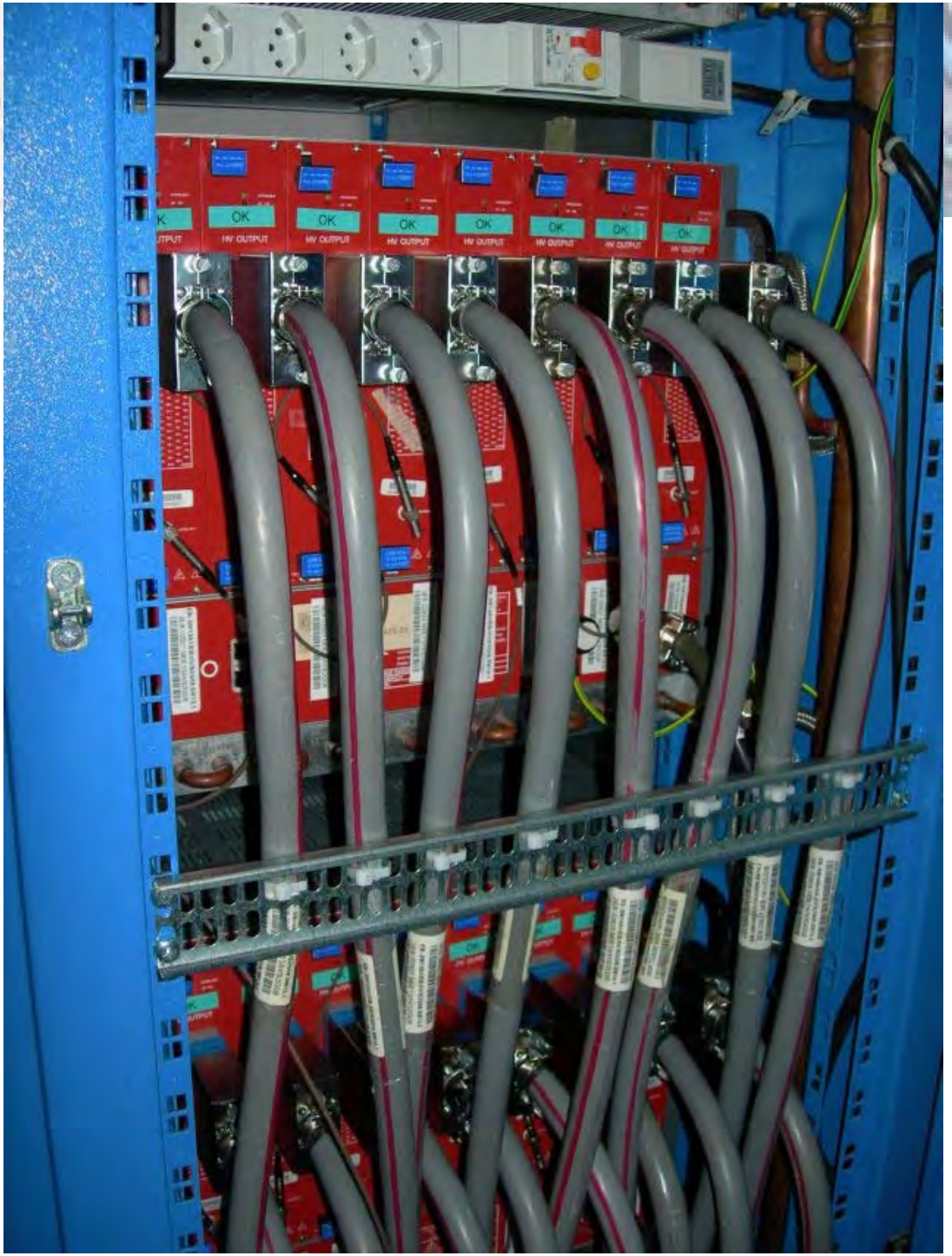

CMS
OWE

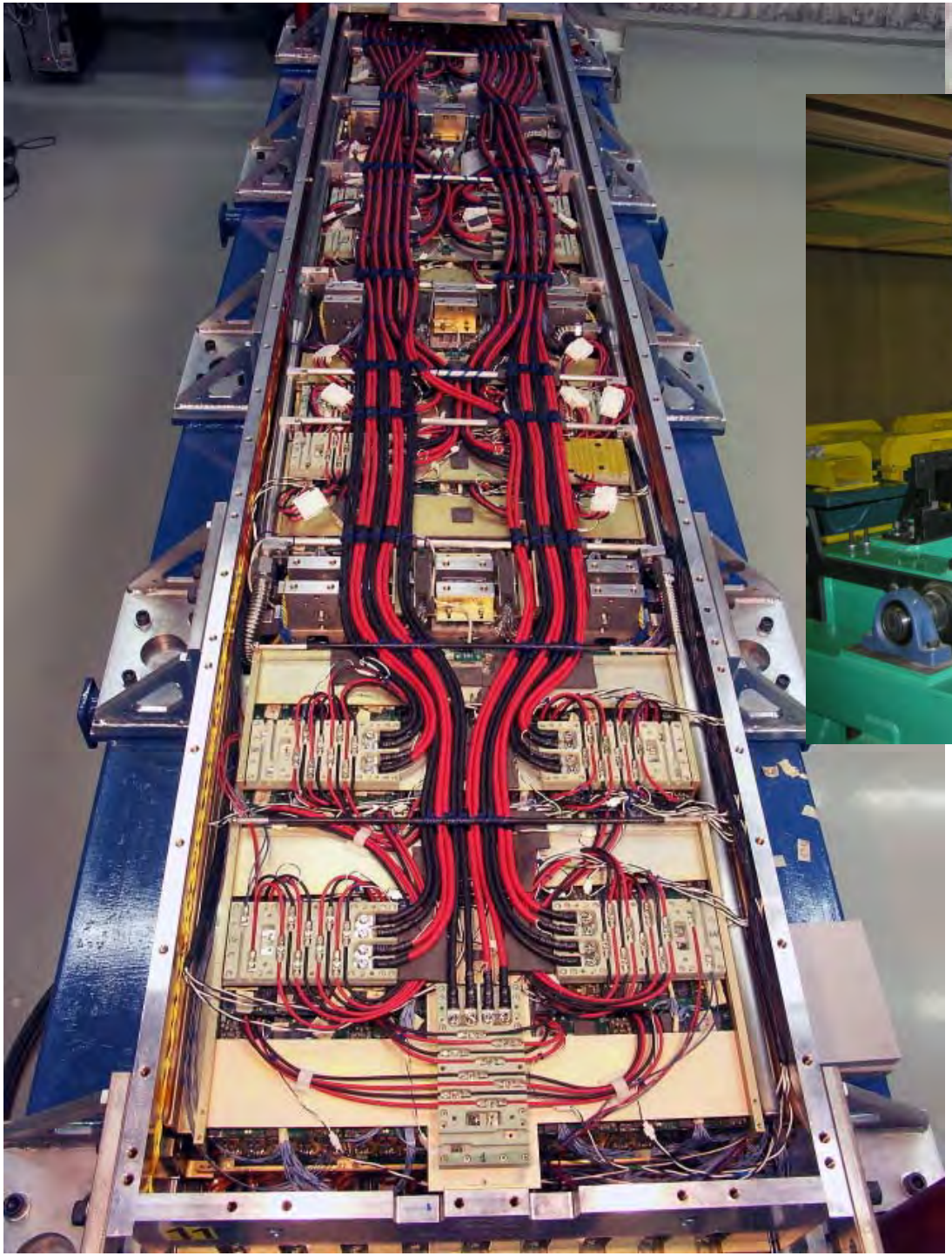

Ansaldo
Superconduttori

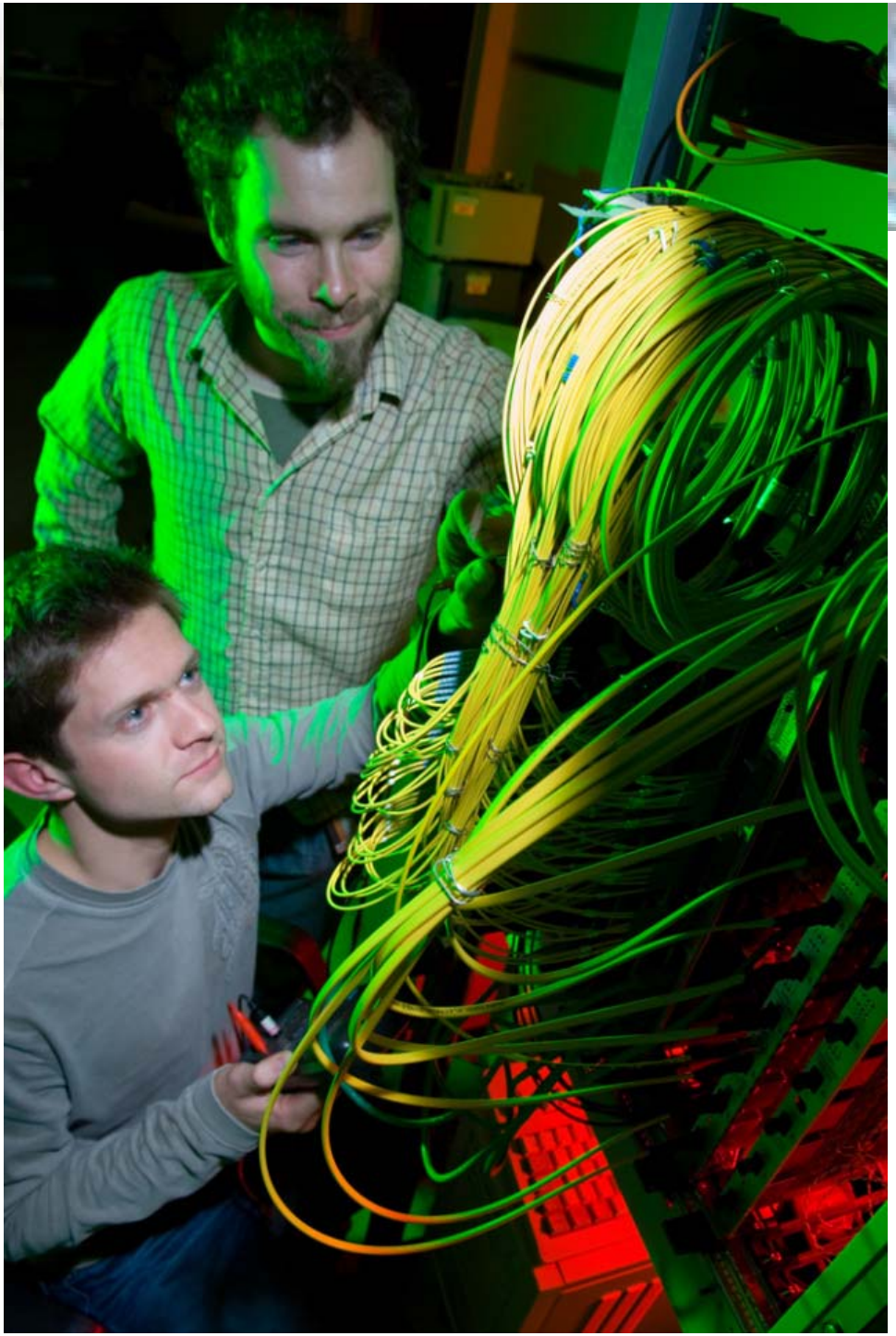



ME+2/2/35
ME+2/2/34




OK
HV OUTPUT





Digital electronics requirements

- While the final design of the backend readout boards (the boards which receive the data digitized by the specialized front-end chips which are digitizing the analog info coming form the detector elements) is not yet available, it is clear what the technology level will have to be for the firms who will get the contract to produce the boards
- These requirements are similar to the one we had for the production of the electronics boards which we are producing for our present 'phase I' upgrade program for the improved trigger, HCAL and Pixel detectors
- In order to evaluate the firms able to compete for the contract a set of questions have been laid down
- From our past experience it has become clear that the questions have to be addressed by the engineers in charge of production, not the 'commercial' representatives: we had to discard several firms which seemed to be qualified once our engineers started talking to the production engineers of the firms
- The memo with the set of questions as well as the detailed specification of one of the boards we have produced recently will be attached to the Agenda.

In summary

- Turkey has contributed very successfully to the construction and realization of the CMS detector we have today and we are convinced that the interests of the Turkish academic community are matched to the technological level of Turkish firms and we are a looking forward to a fruitful collaboration for our future upgrade program as we are convinced that Turkey will contribute successfully in the future as it did in the past

Backup

Questions for electronics firms

1. EXPERIENCE

The firm must have experience of one of the following materials or experience of an alternative material with similar electrical and physical properties; however, we reserve the right to refuse the suggested alternative. The materials below were primarily chosen for (a) low dissipation factor of 0.007 @ 10GHz for reduced attenuation (b) low dielectric constant of 3.2 @ 10GHz enabling 16 layers to be placed in a 1.6mm thick board and (c) lead free processing compatibility.

Nelco N4000-13 SI EP ..... Yes ☐ No ☐

TU872SLK SP ..... Yes ☐ No ☐

The firm must have experience of precise cutting of the PCB from the panel (i.e. to < 0.05mm).

Yes ☐ No ☐

The firm must scale the PCB to an accuracy of better than 0.03%

Yes ☐ No ☐

2. CAPABILITY

The firm must have the capability of rework if required (i.e. ability to replace any part of the board, including the more challenging parts such as LGA).

Yes ☐ No ☐

The firm must have the capability of providing a quality control system that issues a unique identifier to each card, test structure and panel so that card characteristics (e.g. controlled impedance verification), manufacturing information (e.g. reflow profiles) can be retrieved for any card manufactured.

Yes ☐ No ☐

The firm must have experience of assembling cards with the following parts: 0201, 0.4mm pitch surface mount connectors, large BGAs (44x44 pads, 1mm pitch), LGAs (12x12 pads, 1.27mm pitch), QNF, SOIC, etc.

Yes ☐ No ☐

The firm must have the capability of discussing all aspects (sales & technical) in English on a telephone.

Yes ☐ No ☐

3. SUB-CONTRACTING

If any part of the board is to be subcontracted please provide the details (i.e. part to be subcontracted and the name & address of the firm).